CLAIMS

Having thus described our invention in detail, what we claim as new, and desired to secure by the Letters Patent is:

1. A method of forming an interconnect structure including a patterned anti-fuse dielectric layer formed on surface of a substrate, said method comprising the steps of:

(a) forming an anti-fuse dielectric layer on a surface of a substrate, said substrate having a first level of electrically conductive features;

(b) forming an interlevel dielectric layer on said anti-fuse dielectric layer;

(c) forming vias in said interlevel dielectric layer exposing portions of said anti-fuse dielectric layer that overlay said first level of electrically conductive features;

(d) forming a wire level mask on said interlevel dielectric layer, wherein at least of one of said vias and a portion of said interlevel dielectric layer are left exposed;

(e) etching exposed portions of said anti-fuse dielectric layer from said exposed vias, wherein during said etching a portion of said exposed interlevel dielectric layer is removed so as to form a space wherein a second level of

electrically conductive features will be subsequently formed;

(f) stripping said wire level mask; and

(g) filling said vias including said spaces with a conductive material, whereby said second level of electrically conductive features is formed.

2. The method of Claim 1 wherein said first level of electrically conductive features is formed by a single or dual damascene process.

3. The method of Claim 1 wherein step (a) includes a deposition process selected from the group consisting of CVD, plasma-assisted CVD, sputtering and evaporation.

4. The method of Claim 1 wherein said anti-fuse dielectric has a thickness of from about 2 to about 200 nm.

5. The method of Claim 4 wherein said anti-fuse dielectric has a thickness of from about 5 to about 10 nm.

6. The method of Claim 1 wherein said anti-fuse dielectric is a dielectric material selected from the group consisting of SiO_2, Si_3N_4, Si oxynitrides, amorphous Si, amorphous C, H-containing dielectrics, carbon, germanium, selenium, compound semiconductors, ceramics and anti-reflective coatings.

7. The method of Claim 6 wherein said anti-reflective coating is a silicon oxynitride.

8. The method of Claim 1 wherein step (b) includes a deposition process and, optionally, a planarization process.

9. The method of Claim 8 wherein said deposition process is selected from the group consisting of chemical vapor deposition (CVD), plasma-assisted CVD, sputtering, plating and evaporation.

10. The method of Claim 8 wherein said optional planarization process includes chemical-mechanical polishing (CMP) or grinding.

11. The method of Claim 1 wherein said interlevel dielectric has a thickness of from about 0.1 about 2.0 μm.

12. The method of Claim 1 wherein step (c) includes lithography and etching.

13. The method of Claim 1 wherein step (e) includes reactive-ion etching, ion-beam etching or plasma etching.

14. The method of Claim 1 wherein step (g) includes a deposition process.

15. The method of Claim 14 wherein said deposition process is selected from the group consisting of chemical

vapor deposition (CVD), plasma-assisted CVD, sputtering, plating and evaporation.

16. The method of Claim 1 further comprising a planarizing step after step (g).

17. The method of Claim 1 wherein between steps (f) and (g) a barrier layer is applied in said vias and spaces.

18. The method of Claim 1 wherein said vias are slot vias, stacked vias, standard vias or any combinations thereof.

19. The method of Claim 1 further comprising forming additional interconnect levels to said filled structure provided in step (g).

20. The method of Claim 1 further comprising repeating steps (a)-(g) any number of times to provide a multilevel interconnection structure wherein each successive level includes a patterned anti-fuse material formed thereon.

21. The method of Claim 1 further comprising forming a second interlevel dielectric layer on the structure provided in step (g), forming a tapered opening in said second interlevel dielectric level exposing the filled conductive vias and spaces; forming a second conductive material in said tapered opening; and reactive-ion etching said second conductive material.

22. An interconnect structure in which an anti-fuse dielectric is formed therein comprising:

a substrate having a first level of electrically conductive features;

a patterned anti-fuse dielectric layer formed on said substrate, wherein said patterned anti-fuse dielectric layer includes an opening to at least one of said first level of electrically conductive features;

a patterned interlevel dielectric material formed on said patterned anti-fuse dielectric layer, wherein said patterned interlevel dielectric includes vias, as least one of said vias has a via space formed above said opening; and

a second level of electrically conductive features formed in said vias and via spaces.

23. The interconnect structure of Claim 22 wherein said substrate is composed of an interlevel dielectric material that is the same or different from said patterned interlevel dielectric material.

24. The interconnect structure of Claim 22 wherein said patterned interlevel dielectric material is composed of an inorganic semiconductor material selected from the group consisting of SiO_2, Si_3N_4, diamond, diamond-like carbon and fluorinated doped oxides.

25. The interconnect structure of Claim 22 wherein said patterned interlevel dielectric material is composed of an organic dielectric material selected from the group

consisting of polyimides, polyamides, paralyene and polymethylmethacrylate.

26. The interconnect structure of Claim 22 wherein said first and second levels of electrically conductive features are composed of the same or different conductive metal selected from the group consisting of aluminum, tungsten, copper, chromium, gold, platinum, palladium and alloys, mixtures and complexes thereof.

27. The interconnect structure of Claim 22 wherein said anti-fuse dielectric layer is a dielectric material selected from the group consisting of SiO_2, Si_3N_4, Si oxynitrides, amorphous Si, amorphous C, H-containing dielectrics, carbon, germanium, selenium, compound semiconductors, ceramics and anti-reflective coatings.

28. The interconnect structure of Claim 27 wherein said anti-reflective coating is silicon oxynitride.

29. The interconnect structure of Claim 22 wherein another interconnect level is formed over said patterned interlevel dielectric layer.

30. The interconnect structure of Claim 29 wherein said another interconnect level includes a tapered metal contact region.